NAVAL TACTICAL DATA SYSTEM

FUNCTIONAL SPECIFICATION

CHANGE ORDER

NO. ONE

for

TECHNICAL NOTE NO. 240

REPERTOIRE of INSTRUCTIONS

for the

AN/USQ-20 UNIT COMPUTER

PX 1343-36

Remington Rand Univac®
DIVISION OF SPERRY RAND CORPORATION
UNIVAC PARK, ST. PAUL 16, MINNESOTA

NAVY DEPARTMENT | BUREAU OF SHIPS | ELECTRONICS DIVISIONS
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PUBLICATION: *Repertoire of Instructions for the AN/USQ-20 Unit Computer*

PX NUMBER: 1343-36 **REVISION NO:** One **DATE:** 15 February 1961

INSTRUCTIONS: ***Staple Change Order to Document or Enter Revisions in Text.***

Approved: L. D. Findley
L. D. Findley
Manager
Naval Tactical Data System

PAGE	LOCATION	CORRECTION
1	Paragraph 2 line 3	Remove "D" after both "14" and "12"
3	Line 5 from top of page	Remove "D" after "14"
4	Table 1	Add "(OCTAL)" after "CODE" in both instances at the top of Table 1
5	Under "B. *FUNCTION CODE DESIGNATOR* - f", line 4	Replace "00014" with "00000"
	Line 5	Replace "00014" with "00000"
8	Under "H. *MAGNETIC CORE MEMORY ASSIGN-MENT*", line 2	Replace word, "three" with "two" and replace word, "eight" with "seven"
	Line 3	Delete the third line, "1) The starting address from MASTER CLEAR "
9	Lines 1 through 7	Replace "2)" with "1)", "3)" with "2)", "4)" with "3)", "5)" with "4)", "6)" with "5)", "7)" with "6)", and "8)" with "7)"

FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
9	Under "STORAGE FUNCTION" Under ADDRESS 00000: Under ADDRESS 00014: Under ADDRESS 00017:	 Replace "Initial Starting Address from MASTER CLEAR" with "Fault Entrance Register" Replace "Fault Entrance Register" with "Memory Word" Replace "Real-Time Clock Register with "Memory Word"
10	Under "STORAGE FUNCTION" Under ADDRESS 00036: Line 5 Line 6 Line 7 Line 8 Line 9 Line 10 Line 21 Line 22 Line 23 Line 24 Line 25 Line 26	 Replace "Memory Word" with "Real-Time Clock Register" Remove "D" at end of line ↓
11	Line 3 Line 4 Line 5 Line 6 Line 7 Line 8 Line 19 Line 20 Line 21 Line 22 Line 23 Line 24	Remove "D" at end of line ↓
12	Line 1 Line 2 Line 3 Line 4	Remove "D" at end of line ↓

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FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
12	Line 5 Line 6 Under "I. *WIRED MEMORY*" Line 1 Line 2 4th line from bottom of page 2nd line from bottom of page	Remove "D" at end of line Remove "D" at end of line Remove "D" after 16 Remove the second word in the line, "core" Replace "00014" with "00000" Replace "14" with "00"
14	Last line	Remove "D" after "59"
15	Last line	Remove "D" after "59"
16	After "*STORE* C^n" Footnote	Place an asterisk (*) after "*STORE* C^n" Add the following: "*Instruction 17, *STORE* C^n is intended for use in the computer's reply to an interrupt; consequently, it is not synchronized with the input buffering process. Therefore, the execution of *n* sequential Instruction 17's on the same channel, will not place *n* sequential *Input Acknowledge* signals on the *Input Acknowledge* line associated with that channel. It will, in fact, generate a signal which is *n* x 14.8 microseconds wide on that *Input Acknowledge* line. Moreover, it is obvious that the execution of an Instruction 17 on a given channel while an *Input* buffer is in progress on that channel will, in most cases, seriously interfere with the buffered transfer of data. It should be noted however, that any other instruction executed between two Instruction 17's will allow the *Input Acknowledge* line to return to the logical *zero* state for a time consistent with Input/Output specifications before it rises a second time."

FUNCTIONAL SPECIFICATION CHANGE ORDER (Cont.)

PAGE	LOCATION	CORRECTION
20	"53 *SELECTIVE SUBSTITUTE*"	Add the following after the last line in paragraph "In this instruction repeated, K = 0 or K = 4 should not be used."
23	Line 1	Place an asterisk (*) at end of line
	Under "RETURN JUMP (Manual)", line 7	Place an asterisk (*) at end of line
	Footnote	"*This instruction is the normal sequence of events; that is, this sequence occurs when the Return Jump instruction is executed in the context of a program which is proceeding from one instruction to the next by way of skips, jumps, or any programmed branching. However, if the Return Jump immediately follows recognition, by the Control Section of the computer, of an interrupt (that is, if the Return Jump is the instruction stored at the Interrupt Entrance Register), then it must be described as follows: "Store $(P)_p$ in the lower half of memory address Y. Then jump to Y+1." The p-designator controls the modification of (P) and it is set up by the instruction immediately preceding the Return Jump caused by the interrupt. Therefore, the Return Jump causes the storage of the address of the next sequential instruction which would have been executed if the interrupt had not occurred. In fact, the general description of the Return Jump is the latter, with the understanding that, in the non-interrupt case, p is set to *one*, which causes the storing of P+1 in Y."

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